THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 41

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte HIROMICHI YAMADA,
TADASHI FUKUSHIMA,
SHIGERU MATSUO,
TAKASHI MIYAMOTO,
TOORU KOMAGAWA,
and
SYOJI YOSHIDA

_____

Appeal No. 1996-0455
Application No. 07/511,778

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HEARD: JULY 12, 2000

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Before HAIRSTON, BARRETT, and BARRY, Administrative Patent Judges.

HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 1 through 3, 5 through 7, 10 and 11. Claims 4, 8, 9 and 12

have been allowed.

The disclosed invention relates to a graphics processing method and apparatus, and to a microprocessor for executing instructions.

Claims 1 and 11 are illustrative of the claimed invention, and they read as follows:

1. A graphics processing apparatus comprising:

a CPU and a system memory, each connected to a system bus composed of address, data and control buses;

a local memory and a frame memory, each connected to a local bus composed of address, data and control buses; and

a graphics processing processor having a first port connected to said system bus, and a second port connected to said local bus, said graphics processing processor having means for simultaneously accessing said system memory and said local or frame memory via said first and second ports, respectively by simultaneously issuing two separate addresses on respective address buses of said first and second ports.

11. A microprocessor for executing instructions each having a fixed length, comprising:

first instruction holding means for holding a primary instruction read from a program;

second instruction holding means for holding a sub-instruction accompanying said primary instruction; and decoding means for decoding said primary instruction and said sub-instruction, whereby when said primary

instruction is an instruction using said sub-instruction
as a result of decoding of said primary instruction, said sub-instruction held by said sub-instruction holding means is decoded and executed.

The reference relied on by the examiner is:

Katsura et al. (Katsura) 5,046,023
Sept. 3, 1991

Claims 1 through 3, 5 through 7, 10 and 11 stand rejected under 35 U.S.C. § 103 as being unpatentable over Katsura.

Reference is made to the briefs and the answer for the respective positions of the appellants and the examiner.

OPINION

The obviousness rejection of claims 1 through 3, 5 through 7, 10 and 11 is reversed.

With the exception of claim 11, all of the claims on appeal require the simultaneous access of a first memory (e.g., main memory) and a second memory (e.g., frame memory) via two separate ports in the graphics processor. Claim 11 is specifically directed to the decoding of a primary instruction, and to the decoding of a sub-instruction that is used by the primary instruction.

The examiner is of the opinion (Answer, page 3) that Katsura teaches "simultaneous access at column 4, lines 23-31."

Appellants argue (Reply Brief, page 5) inter alia that:

> Further, the above-noted passage of Katsura teaches that an address sent to the second bus is transferred by the bus connection control means (bus switch 20) and the first address bus to the system memory at the same time the first data bus is connected to the second data bus [Figure 1].
>
> Thus it is quite clear that this passage merely teaches the simultaneous occurrence of the transferring of an address from the second bus to the first bus and the connecting of the first data bus to the second data bus so that access can be made to the system memory 12. This passage of Katsura is not concerned with the simultaneous access of system and frame memories via two separate ports as in Appellants' invention.

In short, we agree with appellants' argument that Katsura neither teaches nor would have suggested to one of ordinary skill in the art the simultaneous access of the two memories via two ports of the graphics processor. As a result thereof, the obviousness rejection of claims 1 through 3, 5 through 7 and

10 is reversed.

With respect to the decoding of a primary instruction, and the decoding of a sub-instruction when needed by the primary instruction in claim 11, the examiner has not stated where such instruction decoding can be found in Katsura. The obviousness rejection of claim 11 is, therefore, reversed because of the lack of a prima facie case of obviousness.

DECISION

The decision of the examiner rejecting claims 1 through 3, 5 through 7, 10 and 11 under 35 U.S.C. § 103 is reversed.

REVERSED

KENNETH W. HAIRSTON Administrative Patent Judge	)	
LEE E. BARRETT Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
LANCE LEONARD BARRY Administrative Patent Judge	)	

KWH:hh

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